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TEST STRUCTURE AND METHOD FOR DETERMINING A MINIMUM TUNNEL OPENING SIZE IN A NON-VOLATILE MEMORY CELL

ABSTRACT

A test structure is disclosed for determining the smallest acceptable tunnel opening size in a non-volatile memory cell. Additionally, defect density for one or more tunnel opening sizes may also be determined. In one aspect, the test structure has continuous strips of active area that are used to form a "control" path, a "read" path, and a "write" path. A dielectric layer is formed over the active strips. A one-dimensional array containing a number (N) of same-sized tunnel openings is formed on the write path. A layer of poly silicon is deposited over the dielectric and patterned into strips that are perpendicular to the active strips. The poly silicon strips are aligned with the tunnel openings and form a floating gate and sense device, which is capacitively coupled to external probe pads through the common "control" path. The test structure may have a series of write paths wherein a write path has a one-dimensional array of "N" same-size tunnel openings. The first write path typically includes an array of tunnel openings with a relatively large size, with each additional write path containing an array of tunnel openings of incrementally descending size. The test structure allows bulk (all N gates simultaneously) programming or erasing of any one-dimensional array of a tunnel opening size. Consequently, a large number of same size tunnel openings may be tested in parallel.